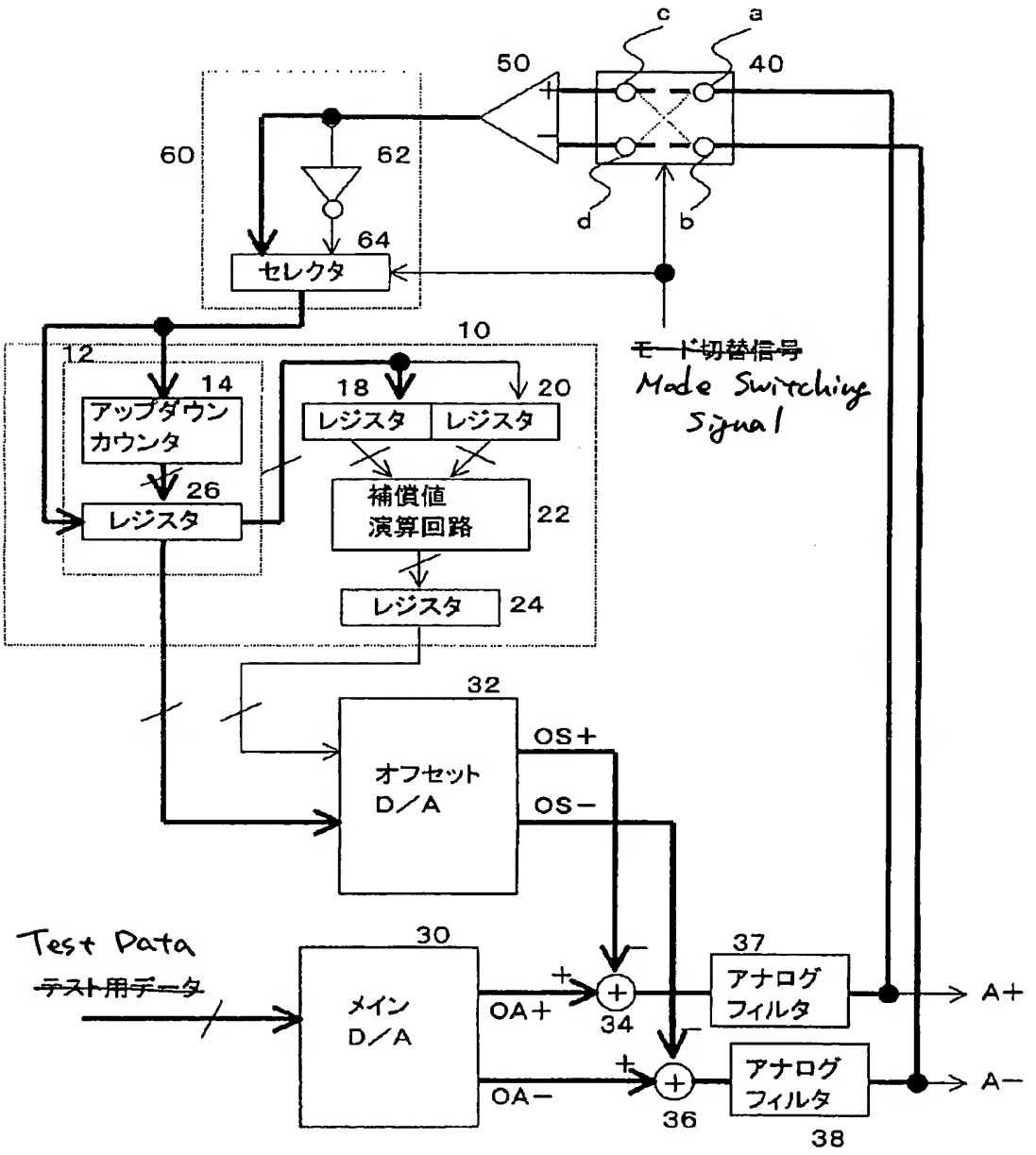
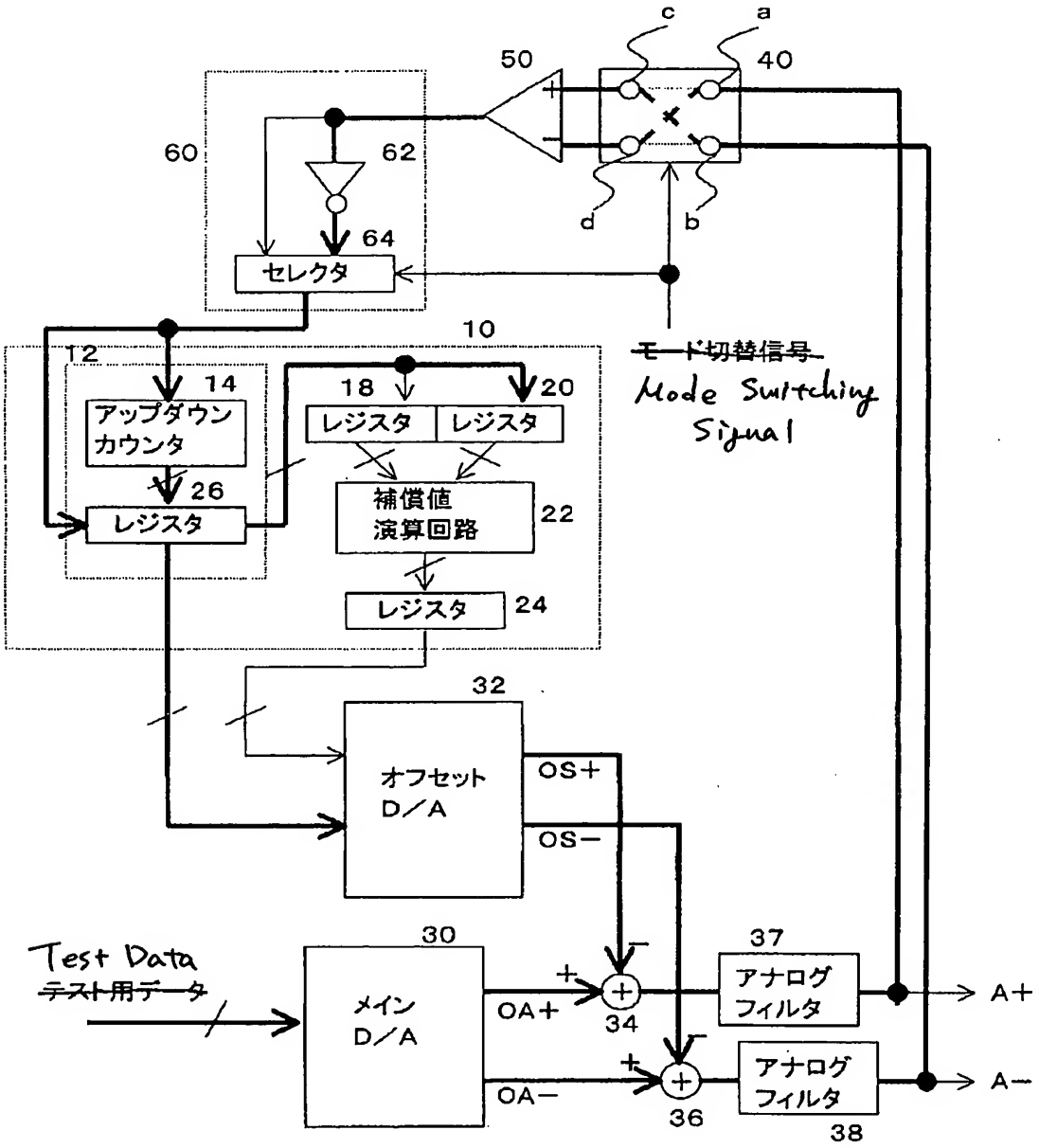
~~【書類名】 図面~~

~~【図1】~~ FIG. 1



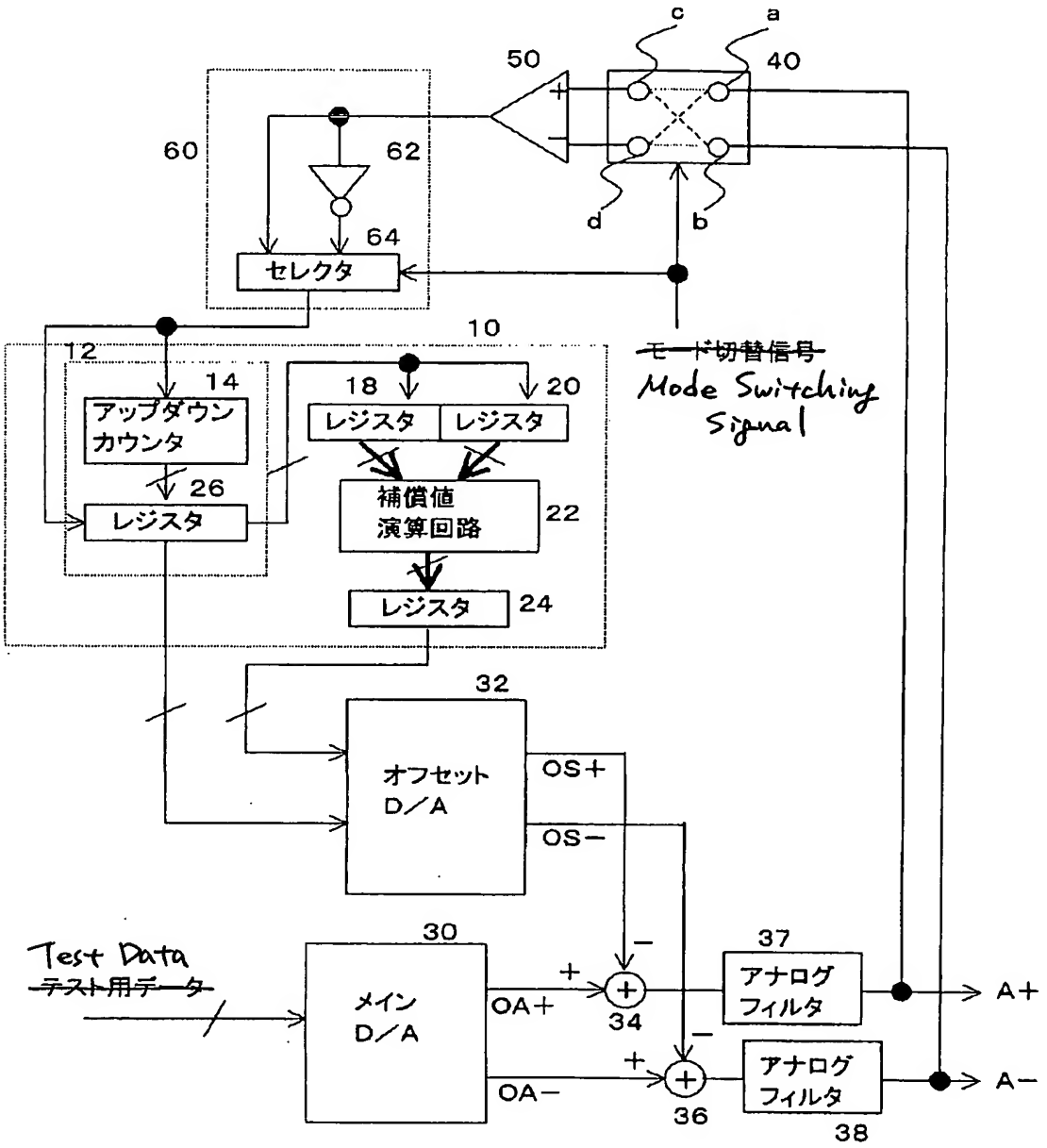
14	Up-Down Counter
18, 20	Register
22	Compensation Value Calculating Circuit
24, 26	Register
30	Main D/A Converter
32	Offset Compensation D/A Converter
37, 38	Analog Filter
64	Selector

~~［図２］~~ FIG. 2



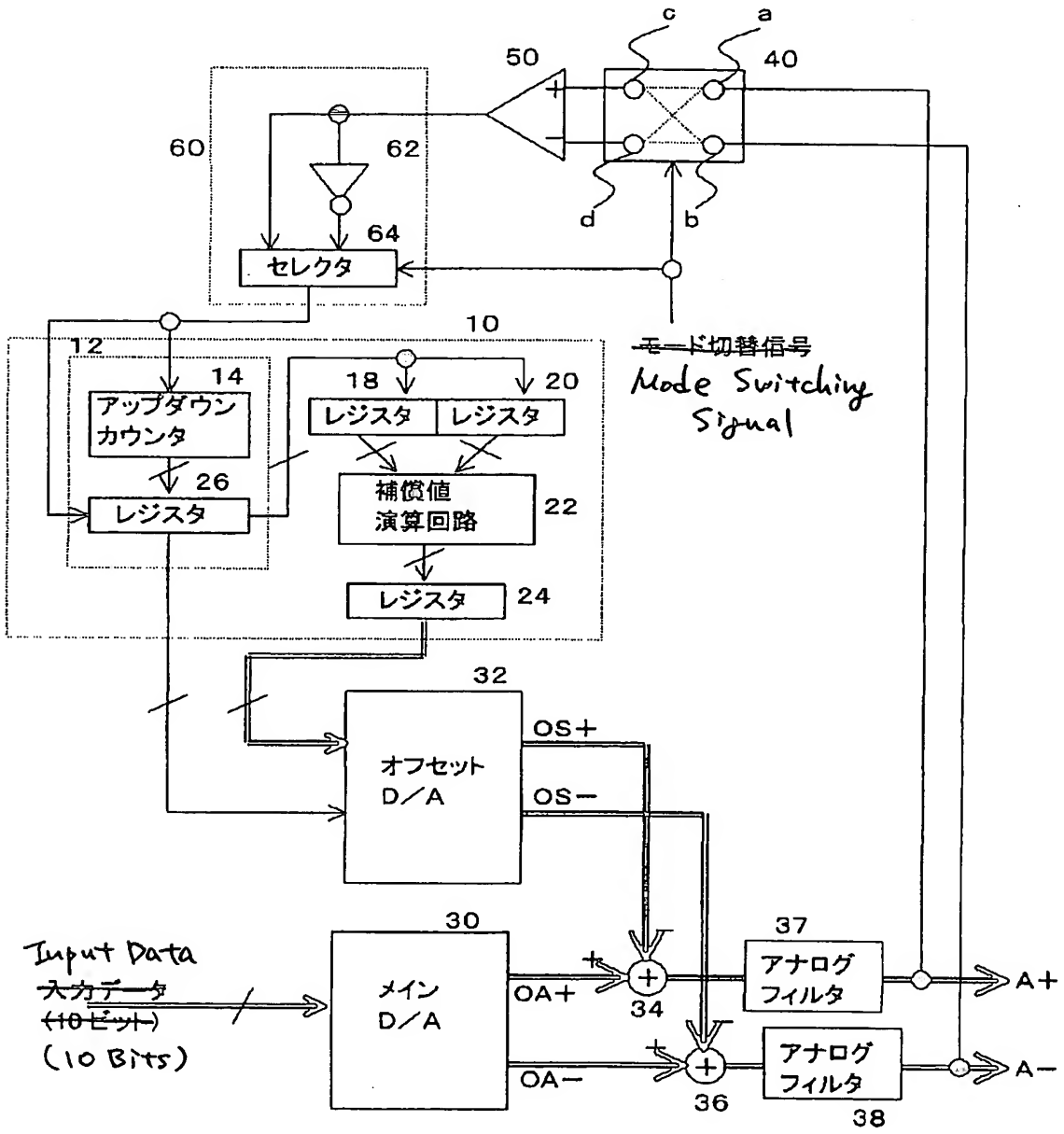
14	Up-Down Counter
18, 20	Register
22	Compensation Value Calculating Circuit
24, 26	Register
30	Main D/A Converter
32	Offset Compensation D/A Converter
37, 38	Analog Filter
64	Selector

~~[図3]~~ FIG. 3



14	Up-Down Counter
18, 20	Register
22	Compensation Value Calculating Circuit
24, 26	Register
30	Main D/A Converter
32	Offset Compensation D/A Converter
37, 38	Analog Filter
64	Selector

~~［図４］~~ FIG. 4



14	Up-Down Counter
18, 20	Register
22	Compensation Value Calculating Circuit
24, 26	Register
30	Main D/A Converter
32	Offset Compensation D/A Converter
37, 38	Analog Filter
64	Selector

~~【図5】~~

FIG. 5A

~~(a)~~

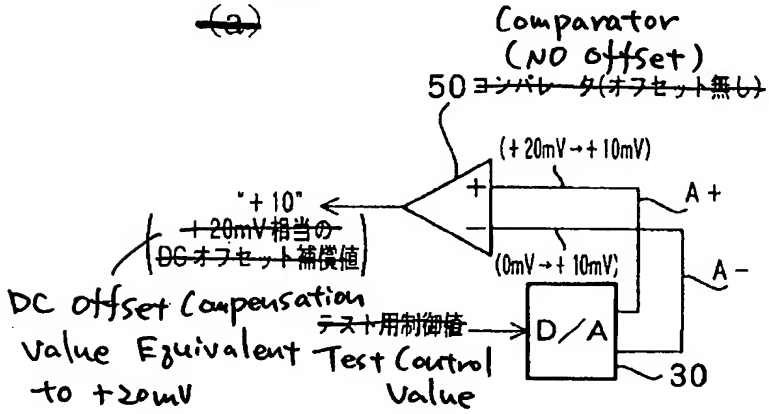


FIG. 5B

~~(b)~~

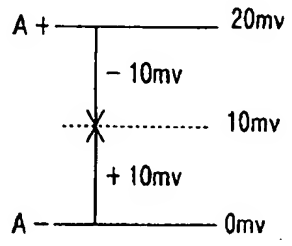
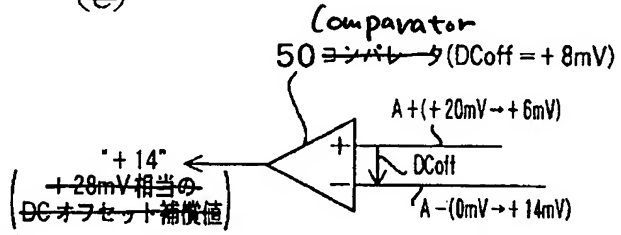


FIG. 5C

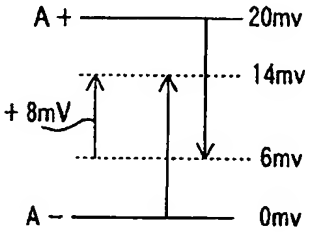
~~(c)~~



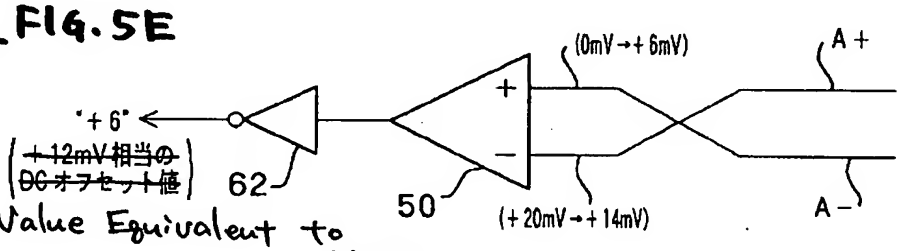
DC offset Compensation Value Equivalent to +28mV

FIG. 5D

~~(d)~~

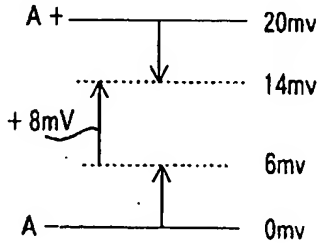


~~(e)~~ FIG. 5E

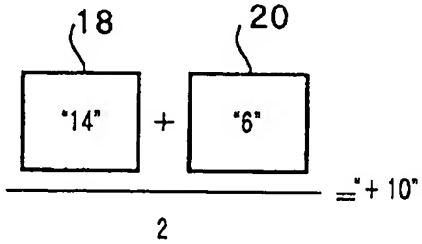


DC offset Value Equivalent to +12mV

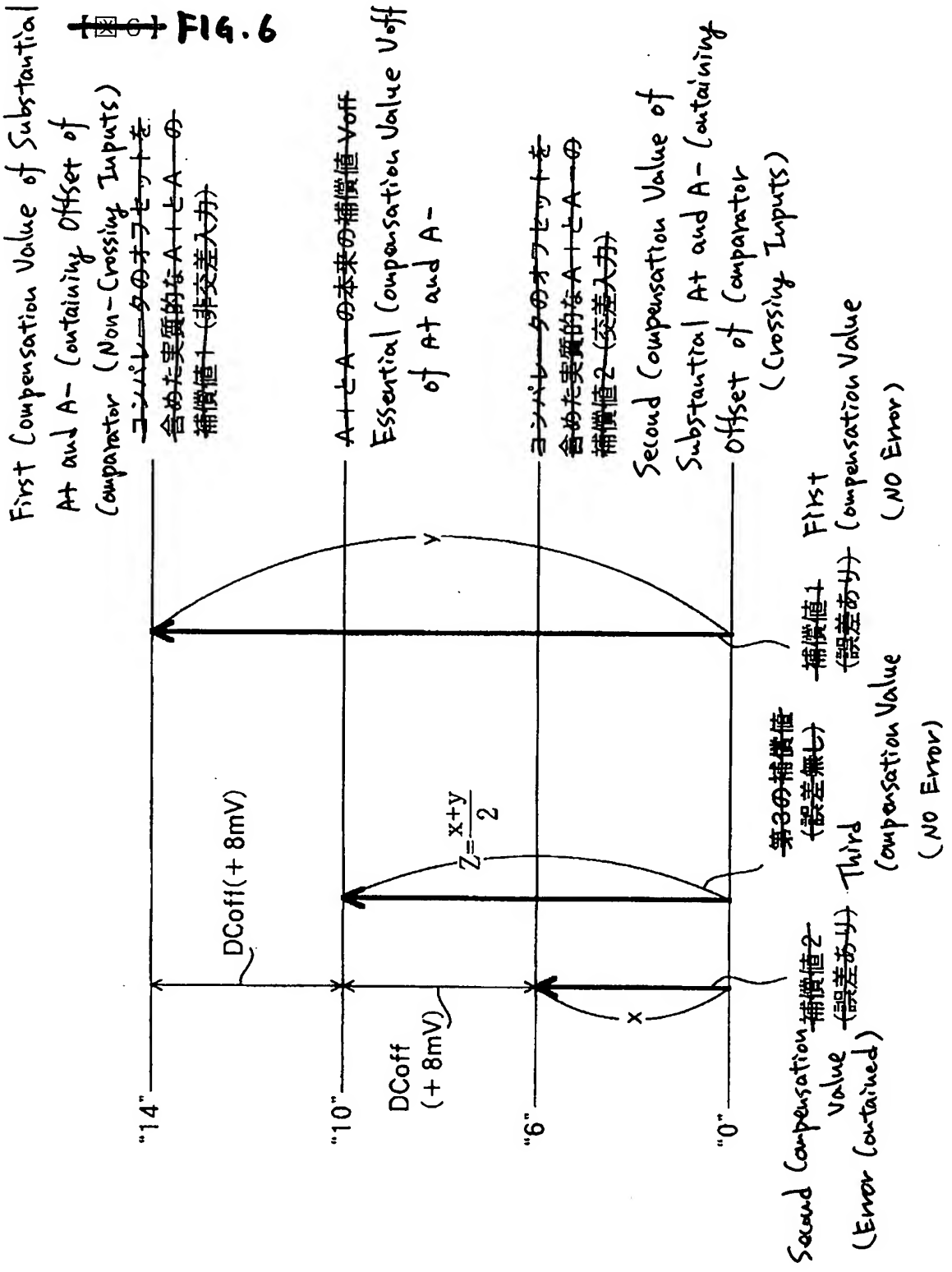
~~(f)~~ FIG. 5F



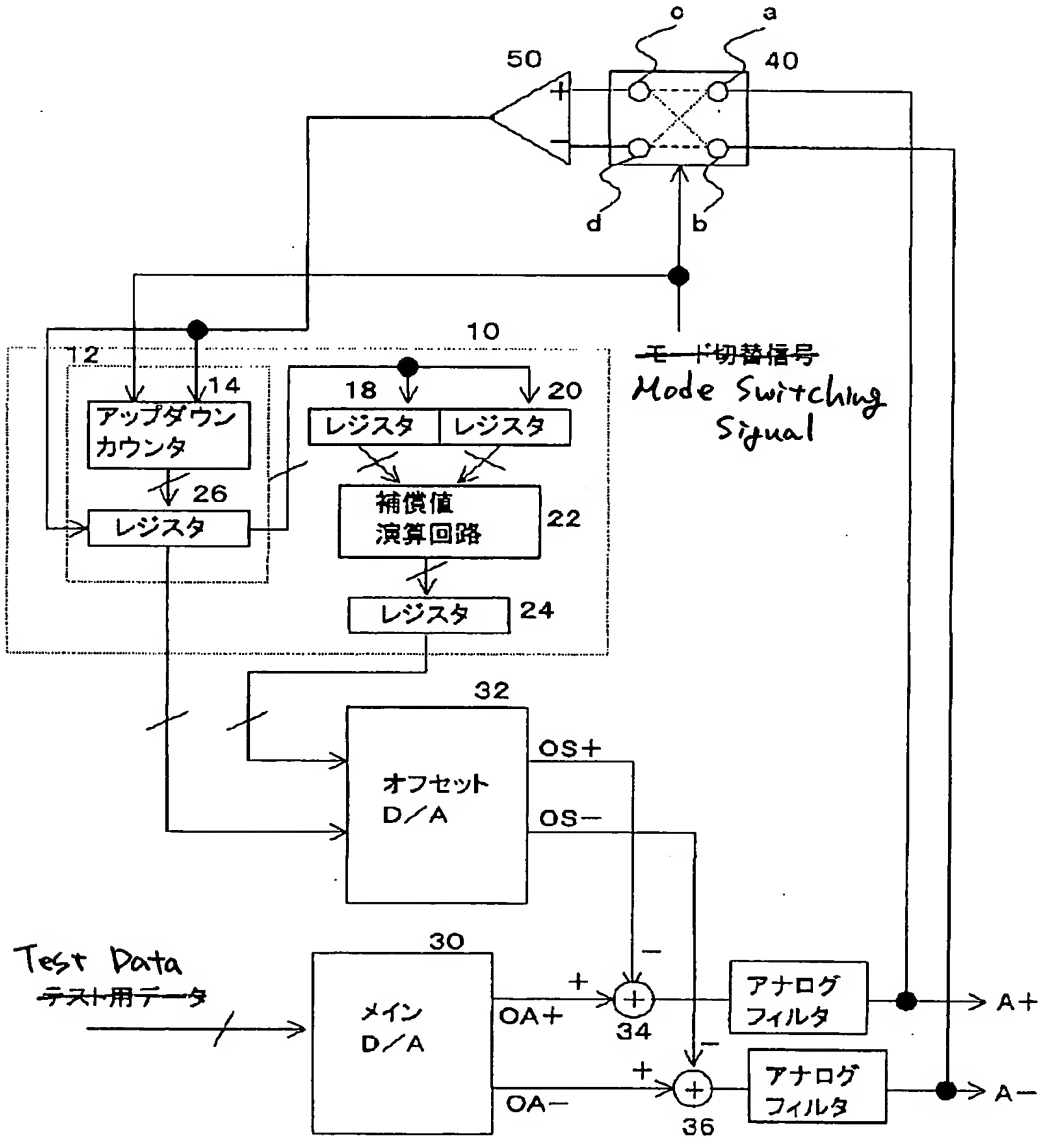
~~(g)~~ FIG. 5G



~~【図6】~~ FIG. 6

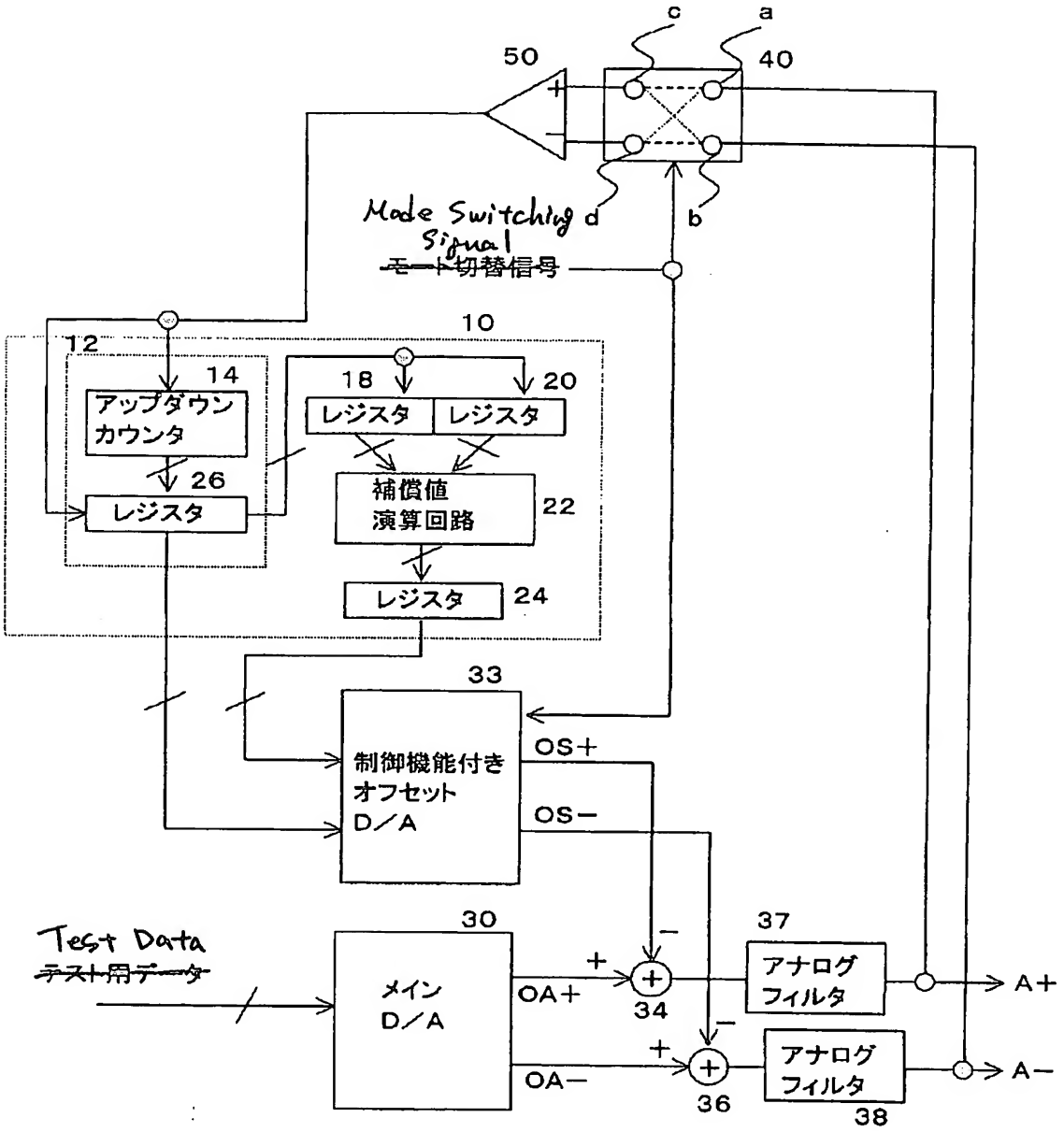

First Compensation Value of Substantial At and A- (containing Offset of Comparator (Non-Crossing Inputs)
コンパレータのオフセットを含めた実質的なA+とA-の補償値1(非交差入力)
A+とA-の本来の補償値Voff
Essential (compensation Value Voff of At and A-
コンパレータのオフセットを含めた実質的なA+とA-の補償値2(交差入力)
Second Compensation Value of Substantial At and A- (containing Offset of Comparator (Crossing Inputs)
Y
DCoff(+8mV)
Z=(x+y)/2
DCoff (+8mV)
X
"14"
"10"
"6"
"0"
第3の補償値(誤差無し)
補償値1(誤差あり)
First (compensation Value (NO Error)
Third (compensation Value (NO Error)
Second (compensation Value (Error contained)
補償値2(誤差あり)

~~［図７］~~ FIG.7



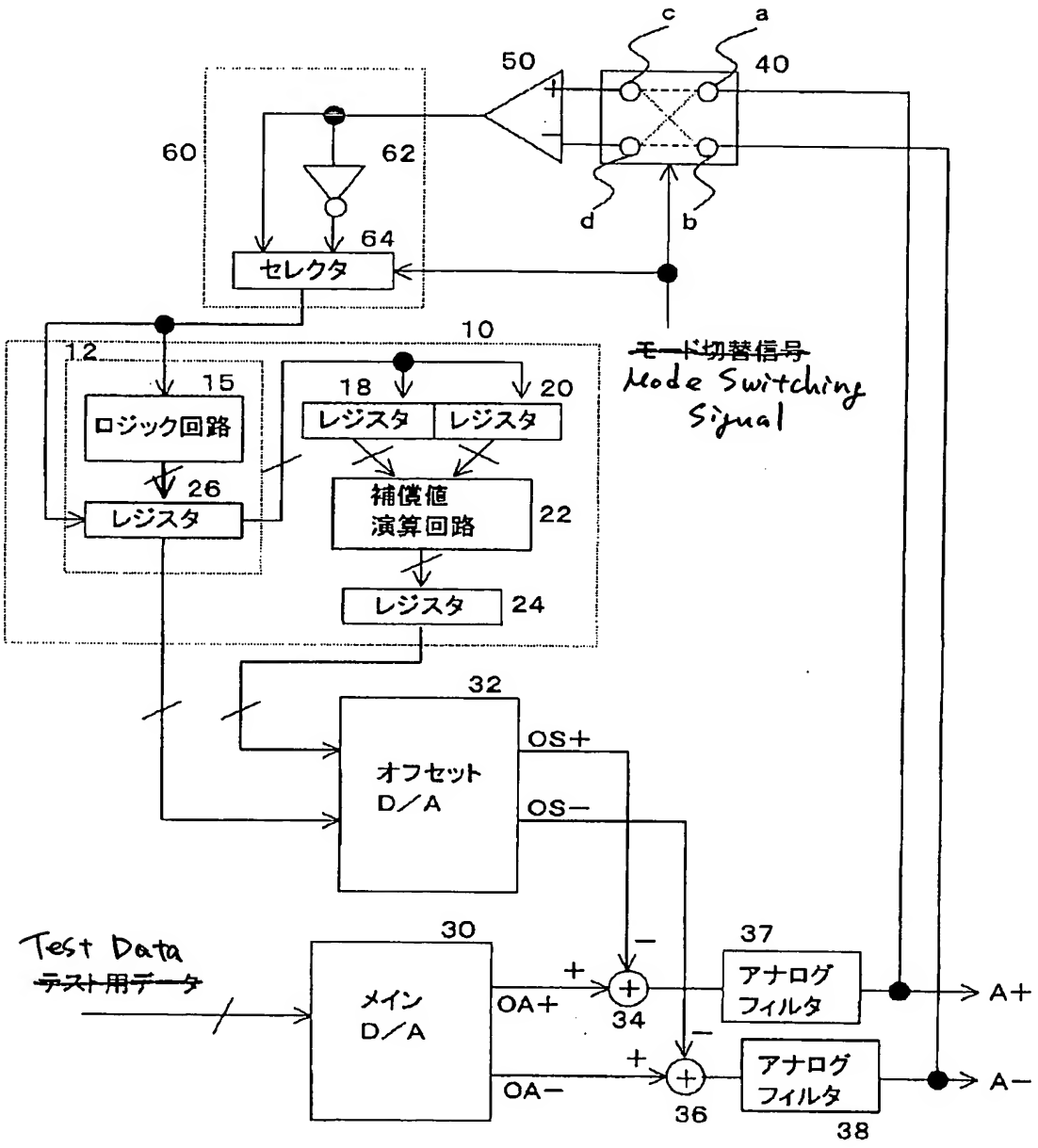
14	Up-Down Counter
18, 20	Register
22	Compensation Value Calculating Circuit
24, 26	Register
30	Main D/A Converter
32	Offset Compensation D/A Converter
37, 38	Analog Filter

~~[図8]~~ FIG. 8



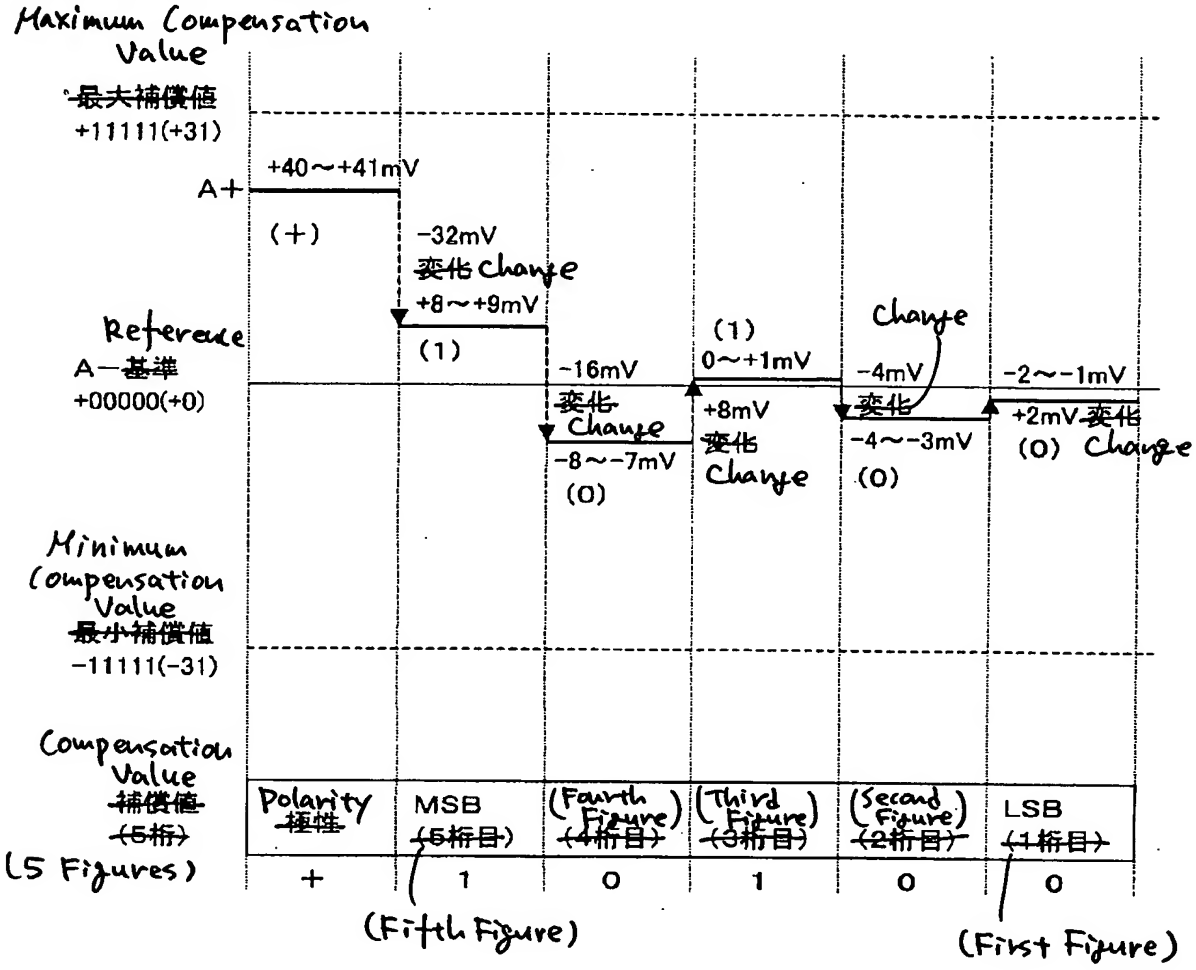
14 Up-Down Counter
18, 20 Register
22 Compensation Value Calculating Circuit
24, 26 Register
30 Main D/A Converter
33 Offset Compensation D/A Converter with Controlling Function
37, 38 Analog Filter

~~［図９］~~ FIG. 9

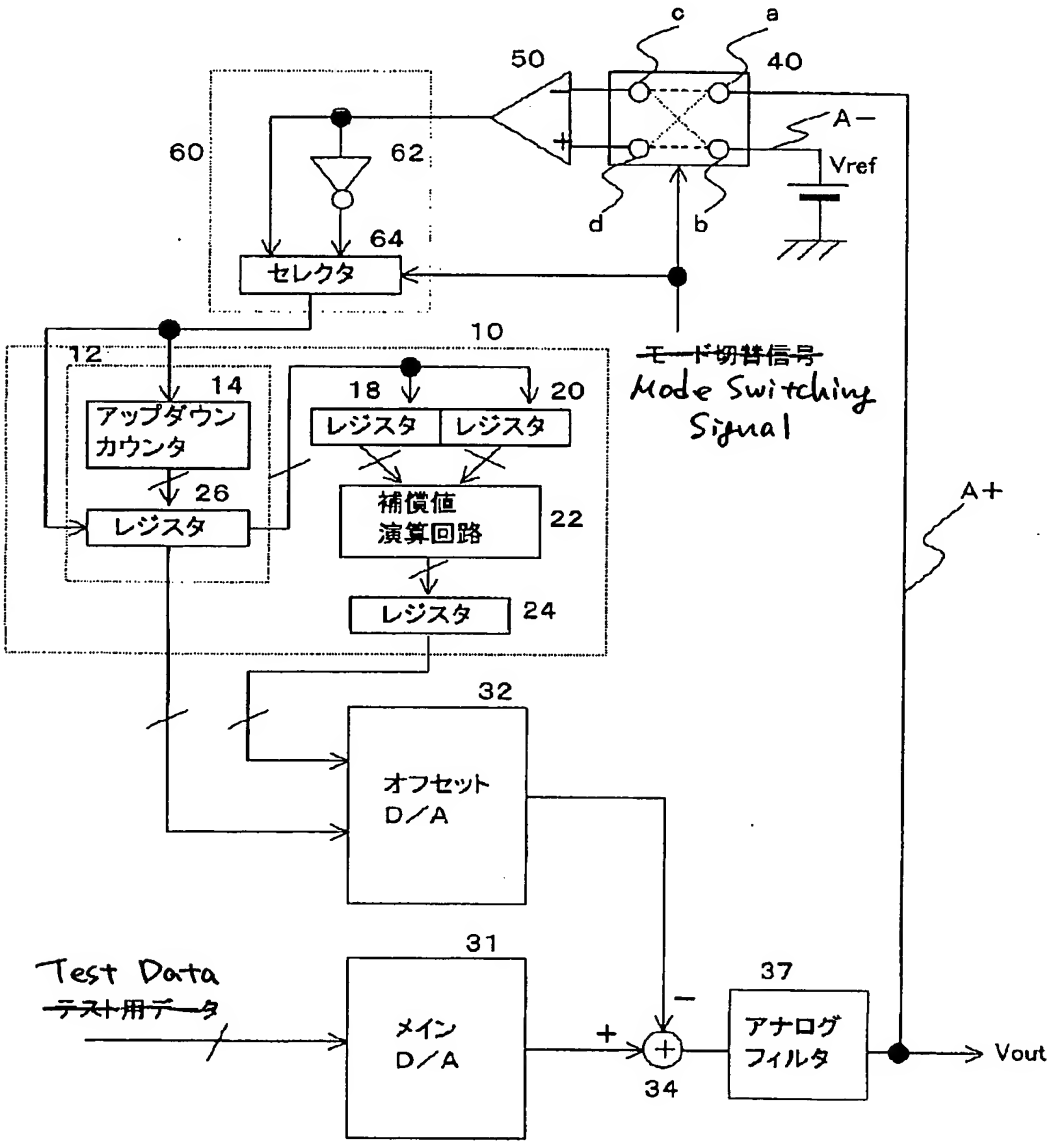


15	Logic Circuit
18, 20	Register
22	Compensation Value Calculating Circuit
24, 26	Register
30	Main D/A Converter
32	Offset Compensation D/A Converter
37, 38	Analog Filter
64	Selector

~~［図10］~~ FIG.10


Maximum Compensation Value
~~最大補償値~~
+11111(+31)
Reference
A－~~基準~~
+00000(+0)
Minimum Compensation Value
~~最小補償値~~
−11111(−31)
Compensation Value
~~補償値~~
~~(5桁)~~
(5 Figures)
A+
+40～+41mV
(+)
−32mV
~~変化~~ Change
+8～+9mV
(1)
−16mV
~~変化~~ Change
−8～−7mV
(0)
(1)
0～+1mV
+8mV
~~変化~~ Change
−4mV
~~変化~~ Change
−4～−3mV
(0)
−2～−1mV
+2mV ~~変化~~ Change
(0)
Polarity ~~極性~~
MSB ~~(5桁目)~~
(Fourth Figure) ~~(4桁目)~~
(Third Figure) ~~(3桁目)~~
(Second Figure) ~~(2桁目)~~
LSB ~~(1桁目)~~
+
1
0
1
0
0
(Fifth Figure)
(First Figure)

~~[図11]~~ FIG.11



14	Up-Down Counter
18, 20	Register
22	Compensation Value Calculating Circuit
24, 26	Register
31	Main D/A Converter
32	Offset Compensation D/A Converter
37	Analog Filter
64	Selector

~~【図１２】~~

FIG.12A
~~(a)~~

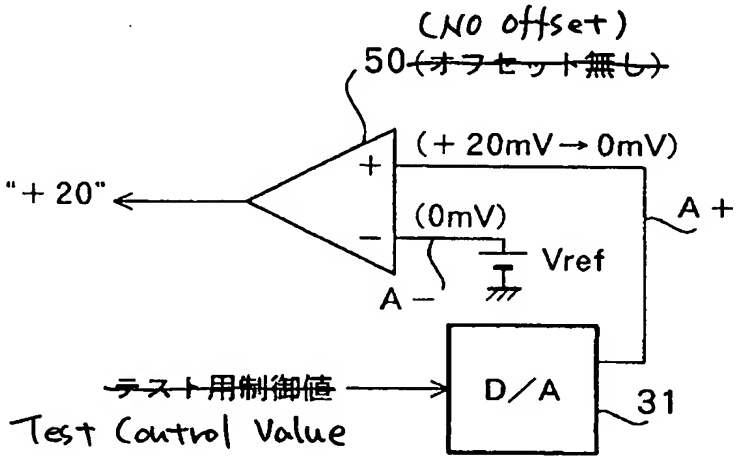


FIG.12B
~~(b)~~

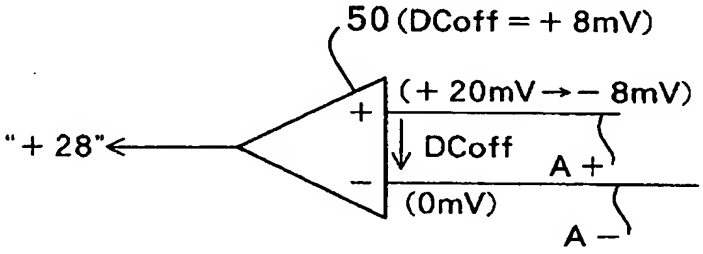


FIG.12C
~~(c)~~

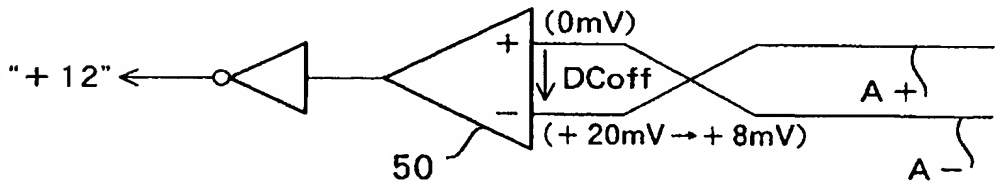
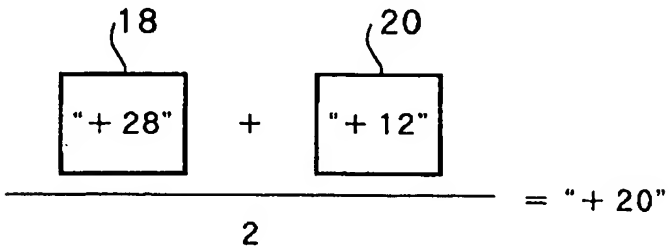
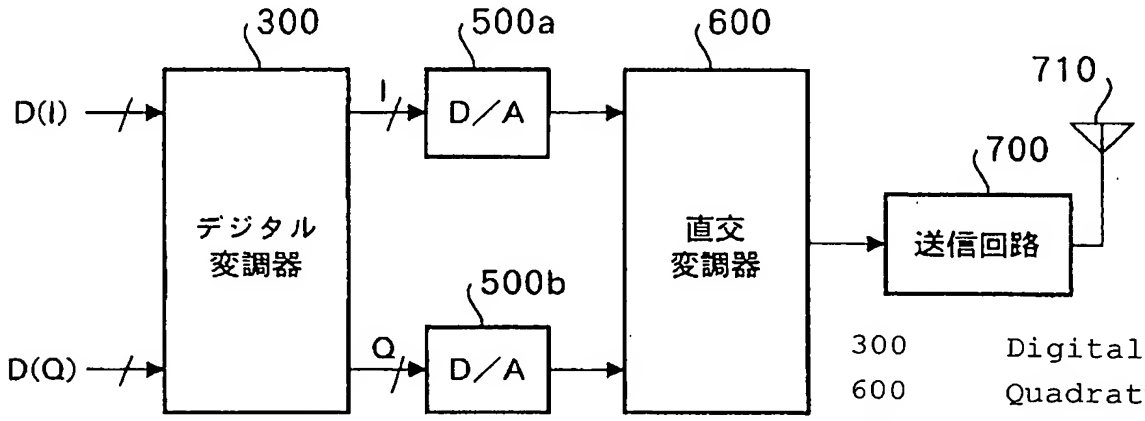


FIG.12D
~~(d)~~



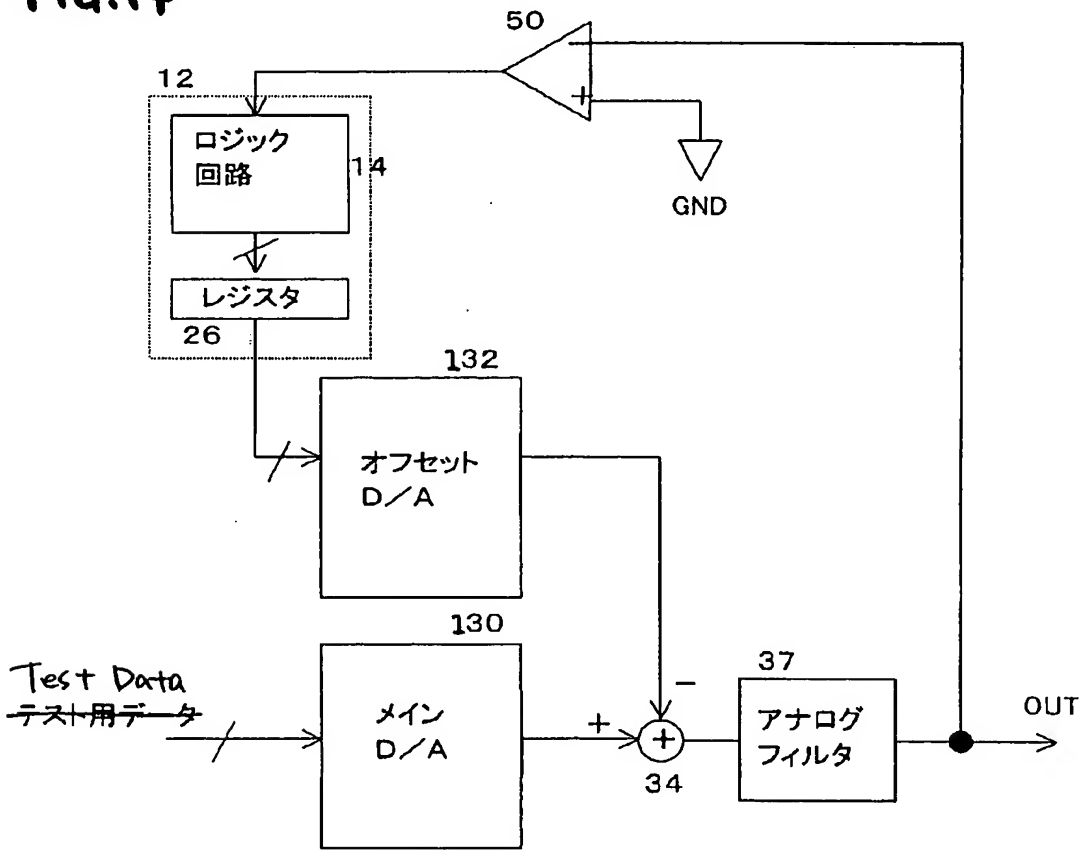
~~[図1-3]~~ FIG.13



300 Digital Converter
600 Quadrature Modulator
700 Transmitting Circuit

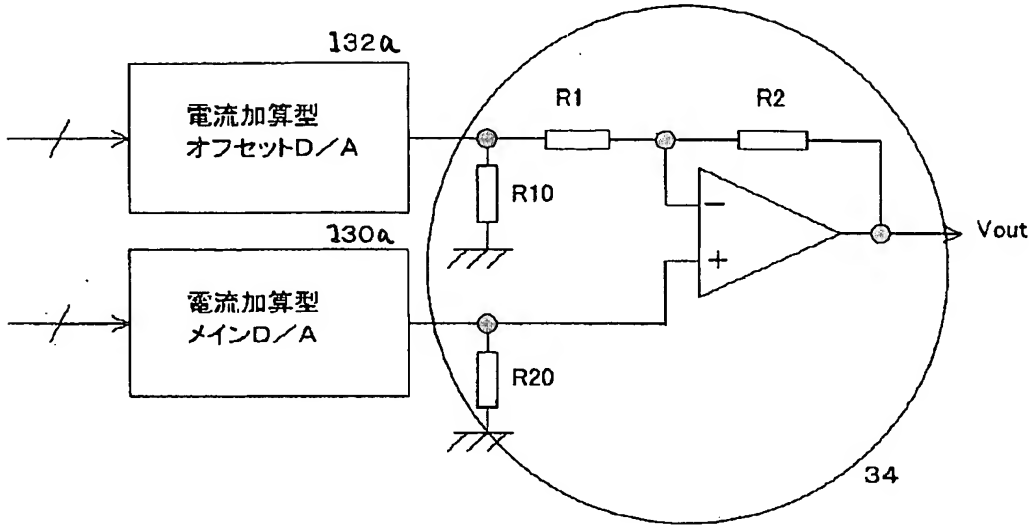
~~[図1-4]~~

FIG.14



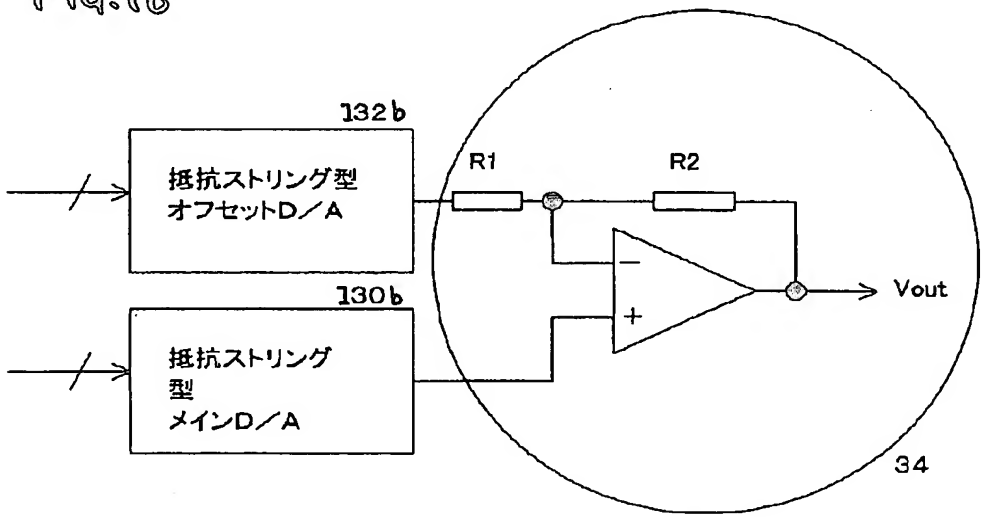
14 Logic Circuit
26 Register
130 Main D/A Converter
132 Offset Compensation D/A Converter
37 Analog Filter

~~[図15]~~ FIG.15



130a Current Summation Type Main D/A Converter
132a Current Summation Type Offset Compensation D/A Converter

~~[図16]~~ FIG.16



130b Resistor String Type Main D/A Converter
132b Resistor String Type Offset Compensation D/A Converter